CLS-222 CAMERA LINK SIMULATOR

# User's Manual

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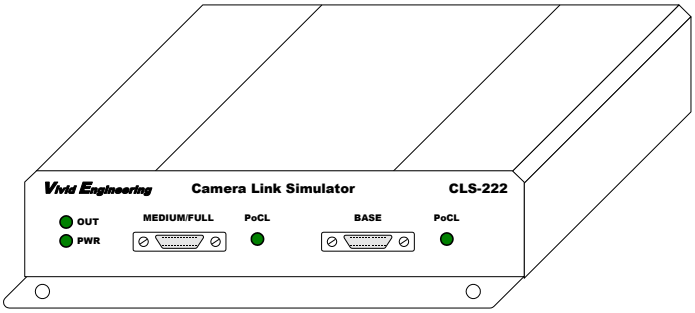
# 1. Introduction

## 1.1. Overview

The CLS-222 Camera Link Simulator is an affordable, high-performance video test pattern generator that supports all video formats including those introduced in Camera Link version 2.1. Fully programmable video timing enables the CLS-222 to mimic the characteristics of almost any camera. New features include enhanced timing performance, bayer color support, and additional video patterns. Control is via an RS-232 port, USB, or frame grabber COM port. The CLS-222 also incorporates the AIA validation test pattern.

The CLS-222 incorporates features for testing and exercising Power Over Camera Link (PoCL) interfaces. The CLS-222 detects power and mimics PoCL camera characteristics at both connectors, supporting newer PoCL cameras. Connectors are the smaller SDR/HDR type typically used with PoCL devices

The CLS-222 is very useful for the development and test of Camera Link components and systems, and is easy to use with included quick-configuration software. The CLS-222 is particularly useful for testing PoCL cables and PoCL frame grabber functionality.



## 1.2. Features

- Supports all Camera Link configurations (base/medium/full/72-bit/80-bit)
- Fully programmable video timing , mimics almost any camera
- Supports all video formats including new Camera Link v2.1
- PoCL power detect at both connectors
- Mimics PoCL camera characteristics
- Video pattern options include wedge, color-bar, and pseudo-random
- Bayer color support
- Area and line scan formats
- "Roll" feature adds pattern motion
- Triggered (exsync) modes
- Supports AIA validation test pattern sequences
- Easy to use with included quick-configuration software. May also be programmed via a command line interface
- Downloadable configuration files are easily created and modified
- Controlled via an RS-232 port, USB (via optional adapter), or frame grabber comm port
- Operates from 10 MHz to 95 MHz, above/below the normal Camera Link 20-85 MHz range for performance/margin testing
- Can operate standalone using stored user configurations
- Sturdy aluminum enclosure w/ mounting flange
- Multi-nation power supply and RS-232 cable included
- Made in USA, 3-year warrantee

## 1.3. Functional Description

The CLS-222 Camera Link Simulator is a programmable video test pattern generator supporting all Camera Link configurations (base, medium, full, 72-bit, 80-bit). All video formats are supported including Camera Link version 2.1. A block diagram is provided in Figure 1-1.

The clock synthesizer, timing generator, and pattern generator functions combine to generate the desired video test image characteristics.

Control of the CLS-222 is via a simple Command Line Interface (CLI). This enables the CLS-222 to be controlled using any computer incorporating a standard RS-232 serial port, or USB using optional adapter. The CLS-222 may also be controlled from the attached frame grabber via the serial communications port that is part of the Camera Link interface. Users may interactively assign settings via the command line interface, or may download configuration files created in advance. Command file generation is simplified using the included Quick Configurator software.

The CLS-222 incorporates non-volatile memory for storing user configuration settings. Saved settings are automatically loaded upon power-up, enabling operation of the CLS-222 using pre-loaded parameters without a host computer.

The CLS-222 clock synthesizer enables the user to select test pattern pixel clock frequencies between 10 and 95 MHz. Note this is beyond the 20-85 MHz range in the camera Link specification and is provided to support performance/margin testing. The camera control inputs of the Camera Link interface are sent to timing generator for use as exsync inputs, enabling the frame grabber to trigger pattern generation if desired. The serial link in the Camera Link interface, when not being used to control the CLS-222, is looped back to the frame grabber enabling loopback test of the serial interface.

The CLS-222 camera interface incorporates the connector, signals, pinout, and chipset in compliance with the Camera Link version 2.1 specification. The CLS-222 incorporates the “base”, “medium”, “full”, “72-bit”, and “80-bit” configuration signal sets, consisting of video data, camera control, and serial communications.

Front panel status LEDs indicate when the unit is powered, and when the CLS-222 is outputting video data. The rear panel incorporates a 4-position mode switch. The mode switch is used to select the controlling interface (RS-232 connector or frame grabber serial port), as well as selecting between up-to 4 user-created configurations.

The CLS-222 is powered by an external multi-nation wall plug-in power supply which is included. Also included is an RS-232 serial cable. An external adapter for controlling the CLS-222 via USB is optional.

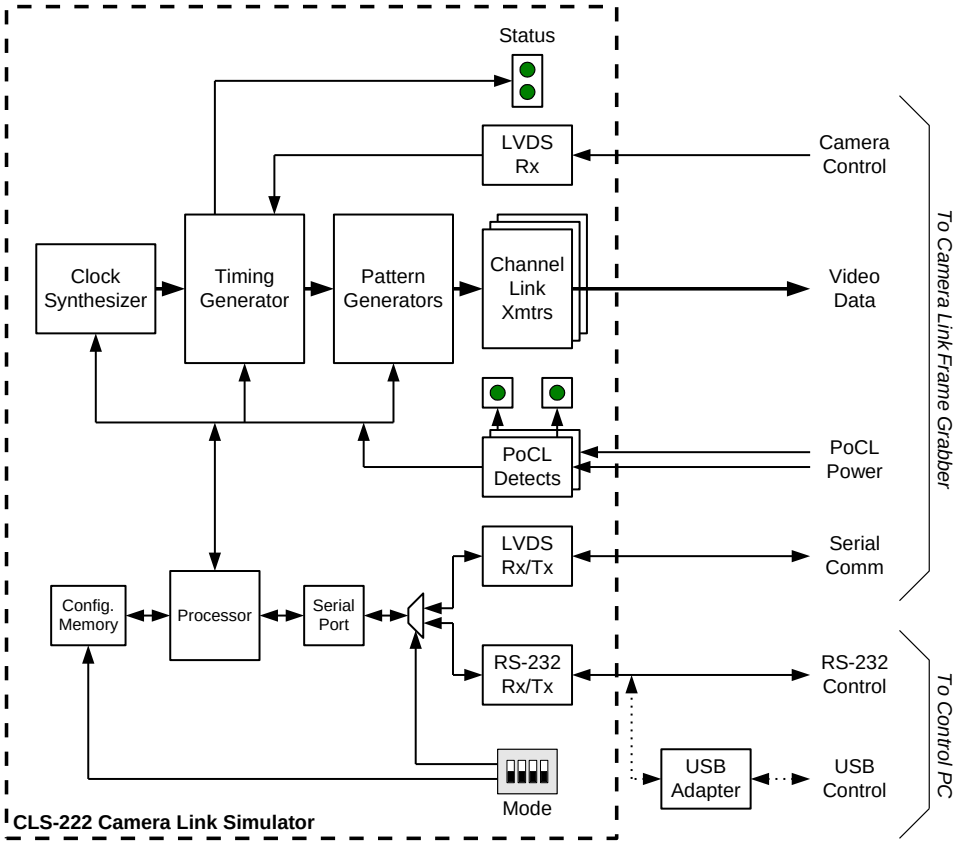



**Figure 1-1: CLS-222 Block Diagram**

### 1.3.1. Timing Generator

The timing generator establishes the basic video timing characteristics by generating the Line Valid (LVAL) and Frame Valid (FVAL) timing signals. The circuit operates at the selected pixel clock frequency.

LVAL is used to envelope *lines* of video data and is defined in the Camera Link specification as *high* for valid line data. Two CLS-222 timing parameters, LVAL_LO and LVAL_HI, determine the duration of LVAL low and high states in pixel clock cycles, respectively. The CLS-222 supports "LVAL low" and "LVAL high" times from 1-65535 pixel clocks. LVAL timing characteristics are shown in Figure 1-2.

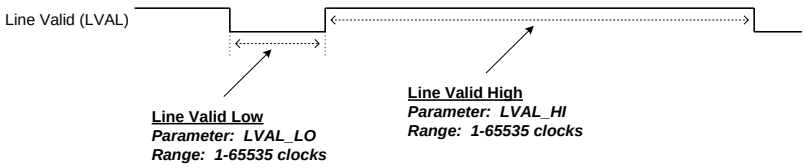



**Figure 1-2: Line Valid (LVAL) Timing Characteristics**

FVAL is used to envelope *frames* of video data from frame scan cameras and is defined in the Camera Link specification as *high* for valid frame data. Two CLS-222 timing parameters, FVAL_LO and FVAL_HI, determine the duration of FVAL low and high states in video lines, respectively. Video lines refer to the Line Valid (LVAL) signal discussed in the last paragraph. The CLS-222 supports FVAL low times of 3-65535 pixel clocks and FVAL high times of 1-65535 lines. FVAL timing characteristics are shown in Figure 1-3.

*Note the minimum FVAL_LO setting is 3.*

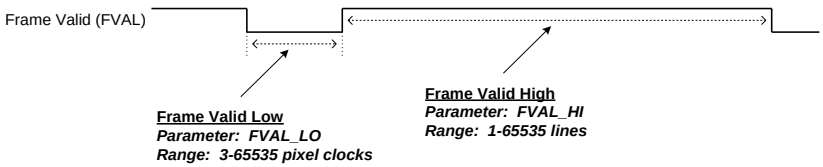



**Figure 1-3: Frame Valid (FVAL) Timing Characteristics**

The relative positioning of the FVAL and LVAL timing signals is programmable and is specified using the Frame Valid Setup (FVAL_SETUP) and Frame Valid Hold (FVAL_HOLD) parameters.

When FVAL_SETUP and FVAL_HOLD are both set to 0, the minimum condition occurs whereby transitions on the FVAL signal occur coincident with the rising edge of the first LVAL in the frame, and the falling edge of the last LVAL in the frame. The FVAL_SETUP value may be increased to provide "setup" time on the FVAL signal prior to the start of the first line in the frame. Similarly, FVAL_HOLD may be increased to provide "hold" time on the FVAL signal following the last line in the frame. This relationship is illustrated in Figure 1-4. The figure is a 2-line frame for illustration purposes.

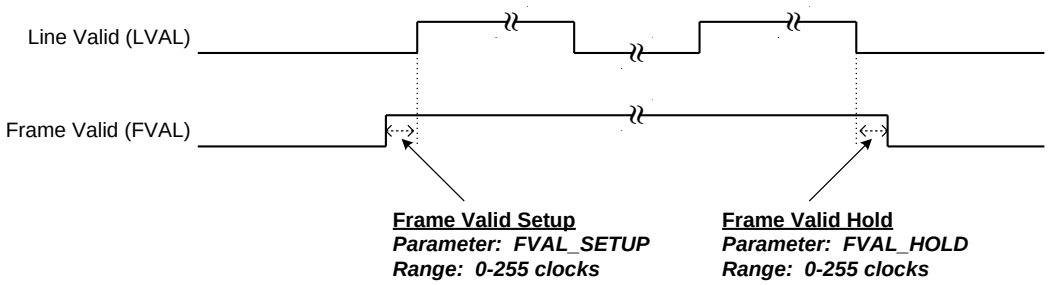



**Figure 1-4: FVAL Setup/Hold Timing Parameters**

### 1.3.2. Pattern Generator

The CLS-222 Camera Link Simulator incorporates a programmable pattern generator to create a variety of test patterns. The CLS-222 is capable of generating fixed-value, horizontal wedge, vertical wedge, diagonal wedge, color bar, pseudo-random, and walking-1 patterns. Example wedge and color bar patterns are shown in Figures 1-5 through 1-8.

Camera Link transmits up-to ten pixels simultaneously (i.e. 8-bit 10-tap mode). The CLS-222 enables the user to select pattern characteristics on a per-pixel basis, denoting the ten pixels A/B/C/D/E/F/G/H/I/J. To support this feature, ten Pattern Select (A_PATSEL, B_PATSEL, C_PATSEL, D_PATSEL, E_PATSEL, F_PATSEL, G_PATSEL, H_PATSEL, I_PATSEL, J_PATSEL) parameters are provided. The PATSEL parameters are defined in Table 1-1.

**Table 1-1: PATSEL Parameter Definition**

| Pattern Select Value (A_PATSEL, B_PATSEL, C_PATSEL, D_PATSEL (E_PATSEL, F_PATSEL, G_PATSEL, H_PATSEL, I_PATSEL, J_PATSEL) | Video Test Pattern |
|---|---|
| 0 | Fixed Value |
| 1 | Horizontal Wedge |
| 2 | Vertical Wedge |
| 3 | Diagonal Wedge |
| 4 | Color Bars |
| 5 | Pseudo-Random |
| 6 | Walking-1 |

For the fixed value pattern, ten Pixel Fixed Value (A_FIXED, B_FIXED, C_FIXED, D_FIXED, E_FIXED, F_FIXED, G_FIXED, H_FIXED, I_FIXED, J_FIXED) parameters are provided to individually select static pixel values.

The CLS-222 provides a selectable pixel step size when generating wedge (horizontal, vertical, diagonal) patterns. The step size determines the amount by which pixel values are incremented from pixel-to-pixel and from line-to-line in the test images. Individual "X" (X_STEP) and "Y" (Y_STEP) settings are provided. The pixel step size feature is particularly valuable for high-resolution (i.e. 12 or 16-bit) video, and with multi-tap formats.

When generating wedge (horizontal, vertical, diagonal) patterns, the CLS-222 enables the user to select the initial value of each pixel. This is the value associated with the first pixel in the video frame. The value then increments, according to the wedge pattern and X/Y step settings. The pixel initial value feature is particularly valuable in generating wedge patterns while simulating multi-tap cameras. Ten Initial Value (A_INIT, B_ INIT, C_ INIT, D_ INIT, E_ INIT, F_ INIT, G_ INIT, H_ INIT, I_ INIT, J_ INIT) parameters are provided.

The CLS-222 "roll" feature used in conjunction with the wedge patterns (horizontal, vertical, diagonal) to introduce test pattern motion. When roll is enabled, the starting pixel value in the video test pattern increments every frame. This changes all pixel values within the pattern every frame and adds a "rolling" motion to the displayed pattern. This feature is particularly useful during testing and for debugging image acquisition problems.

The CLS-222 supports all modes defined in the Camera Link v2.1 specification. The configurations consist of "base", "medium", "full", "72-bit" and "80-bit". These modes range from simple 8-bit single-tap, to complex 80-bit color timeslice formats. The desired mode is selected using the Camera Link Mode (CL_MODE) parameter. The CL_MODE parameter is defined in Tables 1-2 through 1-6.

**Table 1-2: CL_MODE Parameter Definition, 8-bit Pixels**

| CL_MODE Parameter Setting (decimal) | Camera Link Mode (8-bit pixels) |
|---|---|
| 0 | 1-tap mono (base config) |
| 1 | 2-tap mono (base config) |
| 2 | 3-tap mono (base config) |
| 3 | 4-tap mono (med config) |
| 4 | 5-tap mono (med config) |
| 5 | 6-tap mono (med config) |
| 6 | 7-tap mono (full config) |
| 7 | 8-tap mono (full config) |
| 8 | 9-tap mono (72bit config) |
| 9 | 10-tap mono (80bit config) |
| 16 | 1-tap color RGB (base config) |
| 17 | 2-tap color RGB (med config) |
| 18 | 3-tap color RGB (full config) |
| 19 | 1-tap color RGBI (med config) |
| 20 | 2-tap color RGBI (full config) |
| 21 | 1-tap color Bayer (base config) |
| 22 | 2-tap color Bayer (base config) |
| 208 | 10-tap color RGB timeslice (80bit config) |

*Note: "Tap" refers to the number of pixels output at a time…*

**Table 1-3: CL_MODE Parameter Definition, 10-bit Pixels**

| CL_MODE Parameter Setting (decimal) | Camera Link Mode (10-bit pixels) |
|---|---|
| 32 | 1-tap mono (base config) |
| 33 | 2-tap mono (base config) |
| 34 | 3-tap mono (med config) |
| 35 | 4-tap mono (med config) |
| 36 | 5-tap mono (full config) |
| 37 | 6-tap mono (full config) |
| 38 | 7-tap mono (80bit config) |
| 39 | 8-tap mono (80bit config) |
| 48 | 1-tap color RGB (med config) |
| 49 | 2-tap color RGB (full config) |
| 50 | 1-tap color RGBI (med config) |
| 51 | 2-tap color RGBI (80bit config) |
| 52 | 1-tap color Bayer (base config) |
| 53 | 2-tap color Bayer (base config) |
| 209 | 10-tap color RGB timeslice (80bit config) |

*Note: "Tap" refers to the number of pixels output at a time…*

**Table 1-4: CL_MODE Parameter Definition, 12-bit Pixels**

| CL_MODE Parameter Setting (decimal) | Camera Link Mode (12-bit pixels) |
|---|---|
| 64 | 1-tap mono (base config) |
| 65 | 2-tap mono (base config) |
| 66 | 3-tap mono (med config) |
| 67 | 4-tap mono (med config) |
| 68 | 5-tap mono (full config) |
| 69 | 6-tap mono (full config) |
| 80 | 1-tap color RGB (med config) |
| 81 | 2-tap color RGB (full config) |
| 82 | 1-tap color RGBI (med config) |
| 83 | 1-tap color Bayer (base config) |
| 84 | 2-tap color Bayer (base config) |

*Note: "Tap" refers to the number of pixels output at a time…*

**Table 1-5: CL_MODE Parameter Definition, 14-bit Pixels**

| CL_MODE Parameter Setting (decimal) | Camera Link Mode (14-bit pixels) |
|---|---|
| 96 | 1-tap mono (base config) |
| 97 | 2-tap mono (med config) |
| 98 | 3-tap mono (med config) |
| 99 | 4-tap mono (full config) |
| 100 | 5-tap mono (72bit config) |
| 112 | 1-tap color RGB (med config) |
| 113 | 1-tap color RGBI (full config) |
| 114 | 1-tap color Bayer (base config) |

*Note: "Tap" refers to the number of pixels output at a time…*

**Table 1-6: CL_MODE Parameter Definition, 16-bit Pixels**

| CL_MODE Parameter Setting (decimal) | Camera Link Mode (16-bit pixels) |
|---|---|
| 128 | 1-tap mono (base config) |
| 129 | 2-tap mono (med config) |
| 130 | 3-tap mono (med config) |
| 131 | 4-tap mono (full config) |
| 132 | 5-tap mono (80bit config) |
| 144 | 1-tap color RGB (med config) |
| 145 | 1-tap color RGBI (full config) |
| 146 | 1-tap color Bayer (base config) |

*Note: "Tap" refers to the number of pixels output at a time…*

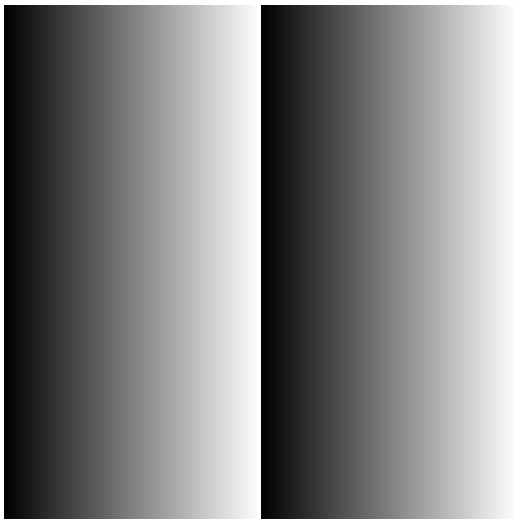


**Figure 1-5: Horizontal Wedge Test Pattern**

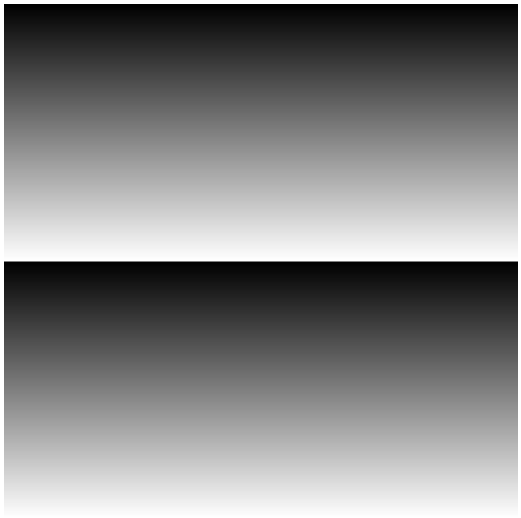


**Figure 1-6: Vertical Wedge Test Pattern**

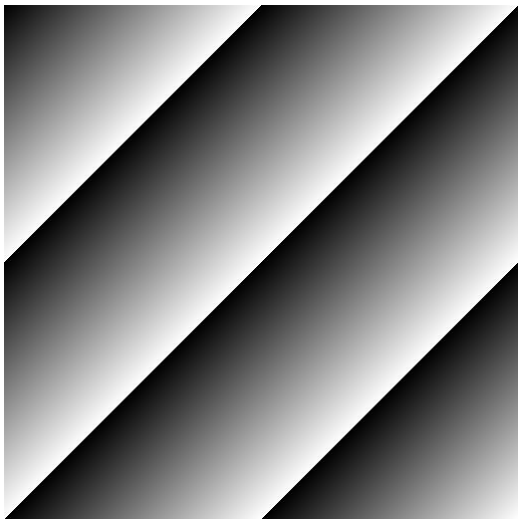


**Figure 1-7: Diagonal Wedge Test Pattern**

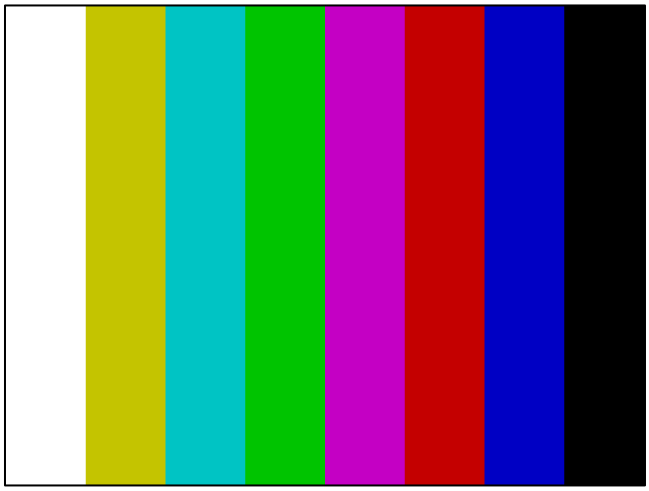


**Figure 1-8: Color Bars Test Pattern**

### 1.3.3. Data Valid (DVAL) Signal

The CLS-222 includes features to mimic low-speed cameras which utilize the Data Valid (DVAL) signal in the Camera Link interface. Camera Link requires a minimum pixel clock rate of 20 MHz. To support cameras and sensors with pixel rates below 20 MHz, the Camera Link interface provides the Data Valid signal which qualifies the data received from the camera. This capability enables a camera to provide a pixel clock of at least 20 MHz, but qualify only a portion of the data sent, effectively providing a sub 20 MHz pixel clock.

The data valid features are controlled using the DVAL and DVAL_MODE control registers. When DVAL_MODE is set to 0, activity on the DVAL signal is disabled and DVAL is held at the static state specified by the DVAL control register. When DVAL_MODE is set to 1-3, the DVAL signal is active (high) every 2nd, 4th, or 8th clock cycle. Data changes occur coincident with the DVAL signal's high-state. The video test pattern data and timing signals from the CLS-222 are automatically replicated (i.e. stalled) for 2/4/8 clock cycles in order to simulate oversampled data coming from cameras that are utilizing the DVAL signal. This is the typical use of DVAL in order to support low pixel clock frequency cameras in Camera Link systems.

See the DVAL and DVAL control register definitions for more information.

### 1.3.4. Configuration Memory

The CLS-222 incorporates non-volatile configuration memory for the storage of user-selected parameters. Upon power-up initialization, the CLS-222 automatically recalls the parameter set stored in memory. This feature enables operation of the CLS-222 without a control port connection. The CLI Parameter Save (SAVE) command is used to store the current parameter set to the configuration memory. The CLI Parameter Recall (RECALL) command configures the CLS-222 using the parameter set currently stored.

The CLS-222 holds up to four user configurations. Selection is via the rear-panel mode switch (see Figure 1-9). Note that the mode switch also selects the CLS-222 control port, RS-232 or frame grabber (i.e. serial port in Camera Link interface).

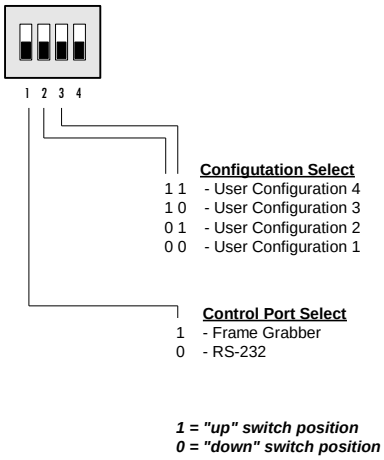



**Figure 1-9: Mode Switch Definition**

### 1.3.5. RS-232 Serial Port

The CLS-222 Camera Link Simulator incorporates a standard RS-232 serial port for linking the CLS-222 to a host PC. The serial port provides RS-232 signal characteristics and incorporates a standard 9-pin D-Sub (DB9) connector. The serial port protocol settings are conventional and are defined in Table 1-3. Connector information is provided in Section 2.2.

**Table 1-3: RS-232 Serial Port Settings**

| Port Characteristic | Setting |
|---|---|
| Rate (bits per second) | 9600 |
| Data Bits | 8 |
| Parity | None |
| Stop Bits | 1 |
| Flow Control | None |

### 1.3.6. USB Support

Alternatively, the CLS-222 Camera Link Simulator may be connected to the host computer USB port using an optional external USB to serial RS-232 adapter. One side of the USB to serial adapter plugs into the PC USB port. The other side of the adapter connects to the RS-232 serial cable included with the CLS-222. Once installed, the PC will create a new serial COM port that may be accessed using the PC in the same fashion as the standard RS-232 serial port. Driver software is included with the USB adapter.

A USB to serial converter is available from Vivid. These converters are also available from computer supply retailers.

### 1.3.7. Camera Control Inputs

The CLS-222 Camera Link Simulator receives four Camera Control (CC1, CC2, CC3, CC4) from the frame grabber as defined in the Camera Link specification. The camera control signal states can be monitored using the CLI, or used as an exsync input to trigger frame/line output.

CLS-222 can be programmed to select a camera control input (CC1, CC2, CC3, or CC4) for use as an exsync trigger. Exsync trigger polarity (rising or falling edge) is also programmable. When configured, the CLS-222 will issue a single frame (or line in linescan mode) in response to each exsync trigger received.

### 1.3.8. Channel Link Transmitters

The CLS-222 Camera Link Simulator incorporates Channel Link transmitter devices for outputting video timing, data, and clock in compliance with the Camera Link v2.1 specification. Three Channel Link transmitter devices are used, one for the "base" connector and two for the "medium/full" connector

Channels not in use are disabled. For instance, in 8-bit single tap mode which is a "base" configuration mode, the "medium" and "full" transmitters are disabled

The Camera Link and device specifications define a 20-85 MHz operating range. CLS-222 is tested to verify an extended operating range of 10-95 MHz. This ability to operate above/below the normal Camera Link range is useful for performance and margin testing.

The Channel Link transmitter chips are authentic Texas Instruments DS90CR287MTD devices per the Camera Link specification.

### 1.3.9. Power over Camera Link (PoCL) Features

The Camera Link Specification includes a version of Camera Link in which power is supplied to the camera via the frame grabber over the Cable Link cable(s). This is known as Power over Camera Link, abbreviated PoCL. Details of the PoCL scheme including an explanation of the SafePower feature, which safely energizes PoCL cameras, are provided in the Camera Link specification.

The CLS-222 incorporates the following features for testing and exercising Power over Camera Link (PoCL) interfaces. These features are particularly useful for testing PoCL cables and PoCL frame grabber functionality:

- Smaller SDR/HDR connectors
- 10K ohm resistive sense loads
- Power presence detectors
- PoCL camera emulation

The CLS-222 incorporates the smaller SDR/HDR connector typically used with PoCL cameras. This facilitates testing both the PoCL frame grabber as well as the PoCL cables used to connect the camera to the frame grabber.

The CLS-222's Camera Link interface includes 10K ohm resistive loads at both the *base* and *medium/full* connectors as specified in the Camera Link specification for PoCL. The CLS-222 will appear as a PoCL camera to frame grabbers that support PoCL. The 10K loads are always present. The CLS-222 does not include a provision to "short" the 10K ohm load which would make the CLS-222 appear to be a non-PoCL camera.

The CLS-222 independently detects 12v power presence from the frame grabber at the *base* and *medium/full* connectors. The threshold voltage for power detection is approximately 10v. PoCL power presence is available to the host computer via the CLI (see PoCL command). Power presence is also shown on the front-panel indicators. The simulator consumes approximately 250mW of PoCL power at each connector.

The CLS-222 mimics both PoCL and non-PoCL cameras. For non-PoCL cameras, the CLS-222 video outputs are enabled regardless of PoCL power presence. To mimic PoCL cameras which are powered through the Camera Link cable(s), CLS-222 video outputs are only enabled when PoCL voltage is detected at either the *base* or the base and *medium/full* connectors (see

POCL_MODE control register). This option enables the CLS-222 to mimic newer PoCL cameras that require power at both connectors. Disabling video output is performed by placing the Texas Instruments DS90CR287MTD transmitter chips in “powder down” mode.

## 1.4. Command Line Interface (CLI)

The CLS-222 is controlled using a simple Command Line Interface (CLI). The CLI may be accessed via standard terminal emulation software (Tera Term, Putty, Hyperterminal, serial port in MATLAB, etc). There is also a terminal window in the included Quick Configurator software.

Upon power-up, the CLS-222 performs a brief system initialization and will respond with the following message:

```
CLS-222 Camera Link Simulator
Command Line Interface (CLI)
Vivid Engineering
Rev 1.0
```

The CLS-222 recognizes the commands defined in the following sections. In the case of invalid syntax, the CLS-222 responds:

```
invalid
```

Accepted write commands receive the following response:

```
ok
```

Sequences of commands are easily created with a text editor (i.e. ".txt" files), saved, and downloaded as desired into the CLS-222. Similarly, current CLS-222 configuration is visible via a DUMP command and can be copied and stored to a file. The included Quick Configurator includes "buttons" for reading and writing configuration files. Spaces, tabs, and returns may be inserted as desired for readability. Comments are indicated using a backslash "/" and may be located at the start of a line or following a command. The following is an example of comments located in a configuration file. Note that numeric information may be entered in either decimal or hexadecimal (0x…) format. An example configuration file is found in Section 1-5.

```
//   Camera Link Configuration File
/    - valid syntax examples
LVAL_HI     500         // decimal notation
LVAL_LO     0x0020      /  hexadecimal notation
Fval_lo     100         // upper or lower case
OK
```

The included Quick Configuration software (Windows XP,7,8,10) is shown in Figure x.x and features an easy-to-use GUI for selecting test image characteristics. The GUI automatically generates the corresponding CLI command set. The command set may be sent to a file, or directly to the CLS-222

device. The Quick Configurator is very useful for "getting started" quickly. Configuration files created using Quick Configurator are easily edited to "fine tune" the CLS-222 commands as needed.

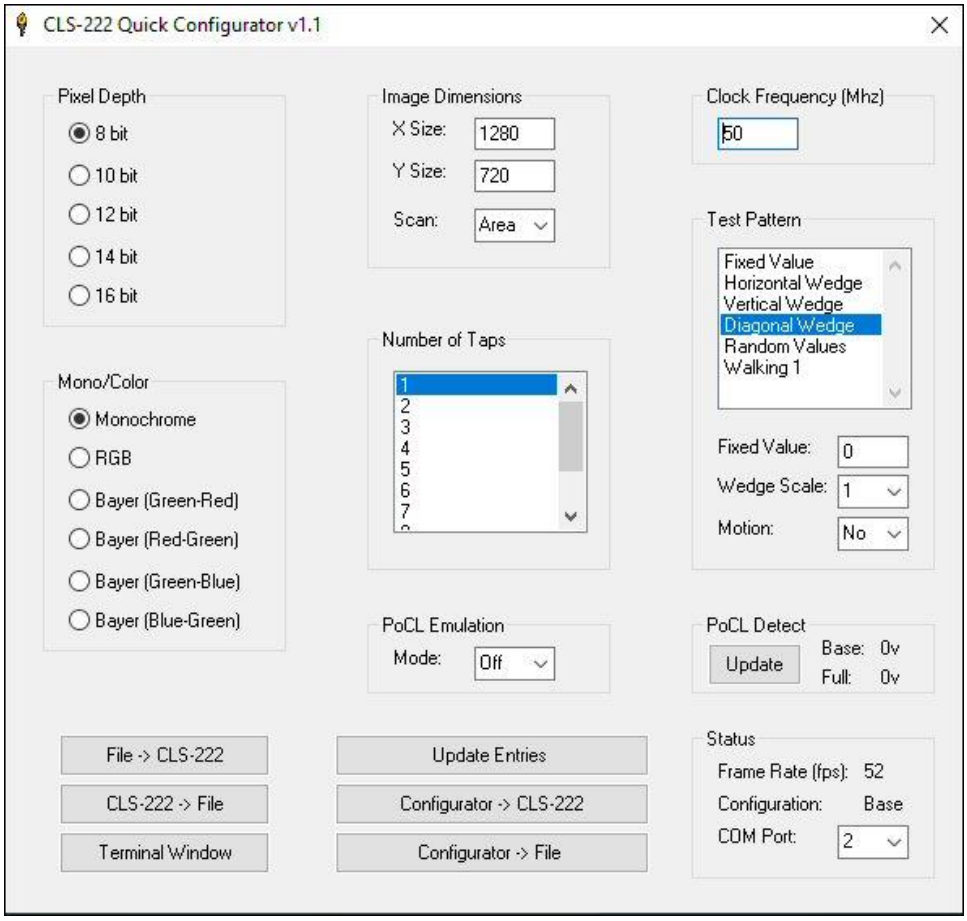



**Figure 2-1: Quick Configurator GUI**

The CLS-222 command set is defined in the following sections.

### 1.4.1. Camera Link Mode (CL_MODE)

The Camera Link Mode (CL_MODE) command determines the test pattern pixel format. The CLS-222 generates video test patterns for all Camera Link modes per the v2.1 specification (i.e. base,medium,full,72-bit,80-bit configurations). Note that "taps" refers to the number of pixels sent at a time. See Section 1.3.2 for further information.

Parameter: CL_MODE
Settings:

0 = 8-bit 1-tap mono (base config)
1 = 8-bit 2-tap mono (base config)
2 = 8-bit 3-tap mono (base config)
3 = 8-bit 4-tap mono (med config)
4 = 8-bit 5-tap mono (med config)
5 = 8-bit 6-tap mono (med config)
6 = 8-bit 7-tap mono (full config)
7 = 8-bit 8-tap mono (full config)
8 = 8-bit 9-tap mono (72bit config)
9 = 8-bit 10-tap mono (80bit config)
16 = 8-bit 1-tap color RGB (base config)
17 = 8-bit 2-tap color RGB (med config)
18 = 8-bit 3-tap color RGB (full config)
19 = 8-bit 1-tap color RGBI (med config)
20 = 8-bit 2-tap color RGBI (full config)
21 = 8-bit 1-tap color Bayer (base config)
22 = 8-bit 2-tap color Bayer (base config)
208 = 8-bit 10-tap color RGB timeslice (80bit config)

32 = 10-bit 1-tap mono (base config)
33 = 10-bit 2-tap mono (base config)
34 = 10-bit 3-tap mono (med config)
35 = 10-bit 4-tap mono (med config)
36 = 10-bit 5-tap mono (full config)
37 = 10-bit 6-tap mono (full config)
38 = 10-bit 7-tap mono (80bit config)
39 = 10-bit 8-tap mono (80bit config)
48 = 10-bit 1-tap color RGB (med config)
49 = 10-bit 2-tap color RGB (full config)
50 = 10-bit 1-tap color RGBI (med config)
51 = 10-bit 2-tap color RGBI (80bit config)
52 = 10-bit 1-tap color Bayer (base config)
53 = 10-bit 2-tap color Bayer (base config)

209 = 10-bit 10-tap color RGB timeslice (80bit config)

64 = 12-bit 1-tap mono (base config)
65 = 12-bit 2-tap mono (base config)
66 = 12-bit 3-tap mono (med config)
67 = 12-bit 4-tap mono (med config)
68 = 12-bit 5-tap mono (full config)
69 = 12-bit 6-tap mono (full config)
80 = 12-bit 1-tap color RGB (med config)
81 = 12-bit 2-tap color RGB (full config)
82 = 12-bit 1-tap color RGBI (med config)
83 = 12-bit 1-tap color Bayer (base config)
84 = 12-bit 2-tap color Bayer (base config)

96 = 14-bit 1-tap mono (base config)
97 = 14-bit 2-tap mono (med config)
98 = 14-bit 3-tap mono (med config)
99 = 14-bit 4-tap mono (full config)
100 = 14-bit 5-tap mono (72bit config)
112 = 14-bit 1-tap color RGB (med config)
113 = 14-bit 1-tap color RGBI (full config)
114 = 14-bit 1-tap color Bayer (base config)

96 = 16-bit 1-tap mono (base config)
97 = 16-bit 2-tap mono (med config)
98 = 16-bit 3-tap mono (med config)
99 = 16-bit 4-tap mono (full config)
100 = 16-bit 5-tap mono (80bit config)
112 = 16-bit 1-tap color RGB (med config)
113 = 16-bit 1-tap color RGBI (full config)
114 = 16-bit 1-tap color Bayer (base config)

Type: Read/Write

*Write Example:* **CL_MODE 0**
*Read Example:* **CL_MODE ?**

### 1.4.2. Continuous Mode (CONTINUOUS)

The Continuous Mode (CONTINUOUS) command enables continuous output of video test patterns. When continuous mode is enabled, the CLS-222 outputs continuous video data. When disabled, video pattern data is suspended, awaiting an exsync pulse, software one-shot command, or return to continuous mode.

Parameter: CONTINUOUS
Settings: 0 (0x0) = Continuous Mode Disabled
1 (0x1) = Continuous Mode Enabled
Type: Read/Write

*Write Example:* **CONTINUOUS 1**
*Read Example:* **CONTINUOUS ?**

### 1.4.3. Exsync Enable (EXSYNC_ENB)

The Exsync Enable (EXSYNC_ENB) command enables triggered output of pattern frames (or lines in LINESCAN mode) using the camera control inputs (CC1, CC2, CC3, CC4). The exsync camera control input source and active edge are selected using the EXSYNC_SEL command.

Parameter: EXSYNC_ENB
Settings: 0 (0x0) = Exsync Triggering Disabled
1 (0x1) = Exsync Triggering Enabled
Type: Read/Write

*Write Example:* **EXSYNC_ENB 0**
*Read Example:* **EXSYNC_ENB ?**

### 1.4.4. Exsync Select (EXSYNC_SEL)

The Exsync Select (EXSYNC_SEL) command select which camera control input and active edge is used when generating exsync-triggered video patterns. The CLS-222 supports exsync triggered frame generation using any of Camera Link camera control inputs. The triggering edge is selectable as "rising" (low-to-high transition) or "falling" (high-to-low transition).

| | |
|---|---|
| Parameter: | EXSYNC_SEL |
| Settings: | 0 (0x0) = CC1 rising edge |
| | 1 (0x1) = CC1 falling edge |
| | 2 (0x2) = CC2 rising edge |
| | 3 (0x3) = CC2 falling edge |
| | 4 (0x4) = CC3 rising edge |
| | 5 (0x5) = CC3 falling edge |
| | 6 (0x6) = CC4 rising edge |
| | 7 (0x7) = CC4 falling edge |
| Type: | Read/Write |

*Write Example:* **EXSYNC_SEL 0**
*Read Example:* **EXSYNC_SEL ?**

### 1.4.5. Linescan Mode (LINESCAN)

The Linescan Mode (LINESCAN) command places the CLS-222 in linescan mode. When linescan mode is disabled, the CLS-222 defaults to framescan mode.

| | |
|---|---|
| Parameter: | LINESCAN |
| Settings: | 0 (0x0) = Framescan Mode |
| | 1 (0x1) = Linescan Mode |
| Type: | Read/Write |

*Write Example:* **LINESCAN 0**
*Read Example:* **LINESCAN ?**

### 1.4.6. Clock Frequency (FREQUENCY)

The Clock Frequency (FREQUENCY) command enables the user to select the Camera Link reference clock in the 10-95 MHz range. Note this range is beyond the 20-85 MHz range defined in the Camera Link specification and is useful for margin and performance testing purposes.

Parameter: FREQUENCY
Range: 10-95 MHz
Type: Read/Write

*Write Example:* **FREQUENCY 50**
*Read Example:* **FREQUENCY ?**

### 1.4.7. Line Valid High (LVAL_HI)

The Line Valid High (LVAL_HI) command is used to establish the duration, in clock cycles for the "high" (logic 1) portion of the Camera Link Line Valid timing signal. See Section 1.3.1 for further information.

Parameter: LVAL_HI
Range: 1-65535 clocks
Type: Read/Write

*Write Example:* **LVAL_HI 1280**
*Read Example:* **LVAL_HI ?**

### 1.4.8. Line Valid Low (LVAL_LO)

The Line Valid Low (LVAL_LO) command is used to establish the duration, in clock cycles for the "low" (logic 0) portion of the Camera Link Line Valid timing signal. See Section 1.3.1 for further information.

Parameter: LVAL_LO
Range: 1-65535 clocks
Type: Read/Write

*Write Example:* **LVAL_LO 32**
*Read Example:* **LVAL_LO ?**

### 1.4.9. Frame Valid High (FVAL_HI)

The Frame Valid High (FVAL_HI) command is used to establish the duration, in lines for the "high" (logic 1) portion of the Camera Link Frame Valid timing signal. See Section 1.3.1 for further information.

Parameter: FVAL_HI
Range: 1-65535 lines
Type: Read/Write

*Write Example:* **FVAL_HI 720**
*Read Example:* **FVAL_HI ?**

### 1.4.10. Frame Valid Low (FVAL_LO)

The Frame Valid Low (FVAL_LO) command is used to establish the duration, in clock cycles for the "low" (logic 0) portion of the Camera Link Frame Valid timing signal. **Note the minimum value of 3**. See Section 1.3.1 for further information.

Parameter: FVAL_LO
Range: 3-65535 clocks
Type: Read/Write

*Write Example:* **FVAL_LO 16**
*Read Example:* **FVAL_LO ?**

### 1.4.11. Frame Valid Setup (FVAL_SETUP)

The Frame Valid Setup (FVAL_SETUP) command determines the number of clock cycles that the rising edge of the Camera Link FVAL signal occurs in advance of the rising edge of the LVAL signal for the first line in a frame. When FVAL_SETUP is set to 0, the rising edge of FVAL is coincident with the rising edge of LVAL. See Section 1.3.1 for further information.

Parameter: FVAL_SETUP
Range: 0-255 clocks
Type: Read/Write

*Write Example:* **FVAL_SETUP 8**
*Read Example:* **FVAL_SETUP ?**

### 1.4.12. Frame Valid Hold (FVAL_HOLD)

The Frame Valid Hold (FVAL_HOLD) command determines the number of clock cycles that the falling edge of the Camera Link FVAL signal occurs following the falling edge of the LVAL signal for the final line in a frame. When FVAL_HOLD is set to 0, the falling edge of FVAL is coincident with the falling edge of LVAL. See Section 1.3.1 for further information.

Parameter: FVAL_HOLD
Range: 0-255 clocks
Type: Read/Write

*Write Example:* **FVAL_HOLD 8**
*Read Example:* **FVAL_HOLD ?**

### 1.4.13. DVAL Mode (DVAL_MODE)

The DVAL Mode (DVAL_MODE) command determines the timing characteristics of the Camera Link Data Valid output signal. Settings 1-3 enable the CLS-222 to simulate oversampled (2x,4x,8x) video data which is generally used to support low pixel clock frequency cameras in Camera Link systems. See Section 1.3.3 for further information.

| | |
|---|---|
| Parameter: | DVAL_MODE |
| Settings: | 0 (0x0) = DVAL is a static output per the DVAL command |
| | 1 (0x1) = DVAL asserted (1) every 2nd pixel clock |
| | 2 (0x2) = DVAL asserted (1) every 4th pixel clock |
| | 3 (0x3) = DVAL asserted (1) every 8th pixel clock |
| Type: | Read/Write |

*Write Example:* **DVAL_MODE 0**
*Read Example:* **DVAL_MODE ?**

### 1.4.14. DVAL State (DVAL)

The DVAL State (DVAL) command determines the static state of the Camera Link Data Valid output signal when DVAL_MODE is set to 0. See Section 1.3.3 for further information.

| | |
|---|---|
| Parameter: | DVAL |
| Settings: | 0 (0x0) = DVAL output set to 0 |
| | 1 (0x1) = DVAL output set to 1 |
| Type: | Read/Write |

*Write Example:* **DVAL 1**
*Read Example:* **DVAL ?**

### 1.4.15. Clock Disable (CLK_DIS)

The Clock Disable (CLK_DIS) command provides individual disable control for the clock output signals generated by the Channel Link transmitter chips (i.e. base, medium, full) in the Camera Link interface. When disabled, all associated Camera Link interface signals (i.e. clock + data) are inactive.

Parameter: CLK_DIS
Bit positions: bit 0 = Base transmitter clock output disabled when "1"
bit 1 = Medium transmitter clock output disabled when "1"
bit 2 = Full transmitter clock output disabled when "1"
bit 3-7 = 0
Type: Read/Write

*Write Example:* **CLK_DIS 0**
*Read Example:* **CLK_DIS ?**

### 1.4.16. X Dimension Pattern Step (X_STEP)

The "X" Dimension Pattern Step (X_STEP) command determines the amount by which the pixel value increments for the horizontal and diagonal wedge test patterns from pixel-to-pixel across a line (i.e. as column increments). This feature is particularly useful for multi-tap images and for larger pixel depths (i.e. 14-bit and 16-bit) where settings greater than 1 are desirable. The step is applied to all pixels generated (i.e. A-J). See Section 1.3.3 for further information.

Parameter: X_STEP
Range: 1 - 255
Type: Read/Write

*Write Example:* **X_STEP 1**
*Read Example:* **X_STEP ?**

### 1.4.17. Y Dimension Pattern Step (Y_STEP)

The "Y" Dimension Pattern Step (Y_STEP) command determines the amount by which the first pixel value of a line increments in the vertical and diagonal wedge test patterns from line-to-line (i.e. as lines increments). This feature is particularly useful for multi-tap images and for larger pixel depths (i.e. 14-bit and 16-bit) where settings greater than 1 are desirable. The step is applied to all pixels generated (i.e. A-J). See Section 1.3.2 for further information.

Parameter: Y_STEP
Range: 1 - 255
Type: Read/Write

*Write Example:* **Y_STEP 1**
*Read Example:* **Y_STEP ?**

### 1.4.18. Color Bar Width (BAR_WIDTH)

The Color Bar Width (BAR_WIDTH) command determines the width in pixels of each of the eight bars that make up a color bar pattern. For instance, a single-tap RGB 1280x720 image would display one complete color bar pattern when BAR_WIDTH is set to 160 (i.e. 160x8 = 1280).

Parameter: BAR_WIDTH
Range: 1 - 255
Type: Read/Write

*Write Example:* **BAR_WIDTH 160**
*Read Example:* **BAR_WIDTH ?**

### 1.4.19. Bayer Select (BAYER_SEL)

The CLS-222 supports BAYER color encoding which is a type of Color Filter Array (CFA) used in many color cameras. Bayer array consists of alternating rows of red-green and green-blue filters. When CL_MODE is set to one of the Bayer color modes, BAYER_SEL determines the colors output in the first two pixels of the image as defined below.

| | |
|---|---|
| Parameter: | BAYER_SEL |
| Settings: | 0 = Green - Red |
| | 1 = Red - Green |
| | 2 = Green - Blue |
| | 3 = Blue - Green |
| Type: | Read/Write |

*Write Example:* **BAYER_SEL 0**
*Read Example:* **BAYER_SEL ?**

### 1.4.20. Pattern Roll (ROLL)

The Pattern Roll (ROLL) command adds motion to video test patterns. Roll is used in conjunction with the horizontal, diagonal, or vertical wedge patterns. When ROLL is enabled, the starting pixel value is incremented every frame. This changes all pixel values each frame and adds a "rolling" affect to the video test pattern. When disabled, the wedge test patterns are static (no change from frame to frame). See Section 1.3.2 for further information.

| | |
|---|---|
| Parameter: | ROLL |
| Settings: | 0 = Roll disable |
| | 1 = Roll enabled |
| Type: | Read/Write |

*Write Example:* **ROLL 0**
*Read Example:* **ROLL ?**

### 1.4.21. Pixel "A-J" Pattern Select (x_PATSEL)

Up-to ten pixels (A,B,C,D,E,F,G,H,I,J) are simultaneously output from the CLS-222 depending on CL_MODE setting. Each pixel pattern is user selectable via ten Pattern Select commands (A-J). See Section 1.3.2 for further information.

Parameters: A_PATSEL, B_PATSEL, … J_PATSEL
Range: 0 = Fixed Value
1 = Horizontal Wedge
2 = Vertical Wedge
3 = Diagonal Wedge
4 = Color Bars
5 = Pseudo-Random
6 = Walking-1
Type: Read/Write

*Write Example:* **A_PATSEL 3**
*Read Example:* **A_PATSEL ?**

### 1.4.22. Pixel "A-J" Fixed Value (x_FIXED)

Up-to ten pixels (A,B,C,D,E,F,G,H,I,J) are simultaneously output from the CLS-222 depending on CL_MODE setting. The pattern placed on each pixel is individually selectable via the A-J PATSEL commands. When a PATSEL is set to "fixed", the fixed value found in the corresponding FIXED register is output. See Section 1.3.2 for further information.

Parameter: A_FIXED, B_FIXED… J_FIXED
Range: Depends on pixel depth (i.e. CL_MODE). 0-65535 max.
Type: Read/Write

*Write Example:* **A_FIXED 0**
*Read Example:* **A_FIXED ?**

### 1.4.23. Pixel "A-J" Init Value (x_INIT)

Up-to ten pixels (A,B,C,D,E,F,G,H,I,J) are simultaneously output from the CLS-222 depending on CL_MODE. The A-J INIT commands determine the wedge pattern starting values on a per-pixel basis. This feature is particularly useful for generating wedge patterns with multi-tap formats. See Section 1.3.2 for further information.

Parameter: A_INIT, B_INIT… J_INIT
Range: Depends on pixel depth (i.e. CL_MODE). 0-65535 max.
Type: Read/Write

*Write Example:* **A_INIT 0**
*Read Example:* **A_INIT ?**

### 1.4.24. AIA Test Enable (AIA_TEST)

The AIA Test Pattern (AIA_TEST) command enables the 410-frame LFSR test patterns proposed at the Camera Link Committee for FPGA validation purposes. Four test patterns exist, one for each camera Link configuration (80-bit, base, medium, full). Pattern selection is made using the AIA_SEL command described below. When enabled, the CLS-222 will output the 410-frame pattern in continuous, triggered, or one fashion and at the user selected pixel clock frequency as determined by the following control registers:

```
FREQUENCY
CONTINUOUS
EXSYNC_ENB
EXSYNC_SEL
ONE_SHOT
AIA_SEL
CLK_DIS
```

A "freeze" mode is also provided in which *only* the 1st frame of the 410-frame pattern is output. This single-frame pattern is much easier to acquire and is useful for general functional and performance testing.

**Note that the settings in all other control registers are ignored when AIA_TEST = 1 or 3.**

Parameter: AIA_TEST
Settings: 0 (0x0) = AIA test pattern disabled
1 (0x1) = AIA test pattern enabled (410-frame sequence)
3 (0x3) = AIA test pattern enabled (freeze mode, frame 1 of sequence only)
Type: Read/Write

*Write Example:* **AIA_TEST 0**
*Read Example:* **AIA_TEST ?**

### 1.4.25. AIA Pattern Select (AIA_SEL)

The AIA Pattern Select (AIA_SEL) command selects which Camera Link configuration (base, medium, full, 80-bit) test pattern is issued when the AIA

LFSR validation pattern is being generated (i.e. AIA_TEST = 1). Test patterns for base, medium, and full configurations have been added to the original 80-bit pattern at the request of the Camera Link Committee.

| | |
|---|---|
| Parameter: | AIA_SEL |
| Settings: | 0 (0x0) = 80-bit LFSR pattern |
| | 1 (0x1) = Base configuration LFSR pattern |
| | 2 (0x2) = Medium configuration LFSR pattern |
| | 3 (0x3) = Full configuration LFSR pattern |
| Type: | Read/Write |

*Write Example:* **AIA_SEL 0**
*Read Example:* **AIA_SEL ?**

### 1.4.26. PoCL Mode (POCL_MODE)

The PoCL Mode (POCL_MODE) command controls the simulator PoCL camera emulation feature. This feature is used to mimic PoCL camera characteristics (i.e. no output from camera unless PoCL power present). When enabled, simulator video output occurs only when PoCL power is present at the *base* connector or at *both* connectors as defined below..

| | |
|---|---|
| Parameter: | PoCL_Mode |
| Settings: | 0 (0x0) = PoCL camera emulation disabled |
| | 1 (0x1) = PoCL power required at *base* connector |
| | 2 (0x2) = PoCL power required at *both* connectors |
| Type: | Read/Write |

*Write Example:* **POCL_MODE 0**
*Read Example:* **POCL_MODE ?**

### 1.4.27. PoCL Power Presence (POCL)

The PoCL Power Presence (POCL) command detects power presence at the Camera Link interface from a PoCL frame grabber. Power is independently detected at both the base and medium/full connectors. This register is read only. See Section x.x.x for further information.

| | |
|---|---|
| Parameter: | POCL |
| Settings: | 0 (0x0) = No PoCL power present |
| | 1 (0x1) = PoCL power present at *base* connector |
| | 2 (0x2) = PoCL power present at *full* connector |
| | 3 (0x3) = PoCL power present at *both* connectors |
| Type: | Read |

*Read Example:* **POCL ?**

### 1.4.28. CC State (CC)

The CC State (CC) command is used to read the current state of the Camera Link camera control inputs (CC1,CC2,CC3,CC4). This register is read only. See Section 1.3.7 for further information.

Parameter: CC
Bit positions: bit 0 = CC1 (lsb)
bit 1 = CC2
bit 2 = CC3
bit 3 = CC4
bit 4-7 = 0
Type: Read

*Read Example:* **CC ?**

### 1.4.29. FPGA Version (VERSION)

The FPGA Version (VERSION) command is used to read the hardware version code for the CLS-222 Field Programmable Gate Array (FPGA) device. The standard version code is 17. Note that the firmware version is displayed in the startup messages.

Parameter: VERSION
Settings: 8-bit FPGA version code (17 standard)
Type: Read

*Read Example:* **VERSION ?**

### 1.4.30. One Shot Trigger (ONE_SHOT)

The One Shot Trigger (ONE_SHOT) command enables the triggering of a single frame (or line for linescan mode) via the CLI. Note that continuous mode must be disabled to use this feature (see CONTINUOUS command). There is no read or write data associated with this command.

Parameter: ONE_SHOT
Settings: None, command only
Type: Command

*Example:* **ONE_SHOT**

### 1.4.31. Parameter Save (SAVE)

The Parameter Save (SAVE) command stores the current CLS-222 parameter set to non-volatile memory. Up-to four user configurations can be stored. Selection is via the rear panel mode switch. The saved parameters are recalled automatically following power-up, or in response to the RECALL command. Saved parameters are maintained until altered via a subsequent SAVE command. There is no read or write data associated with this command.

Parameter: SAVE
Settings: None, command only
Type: Command

*Example:* **SAVE**

### 1.4.32. Parameter Recall (RECALL)

The Parameter Recall (RECALL) command retrieves parameter sets currently stored in non-volatile memory. Up-to four user configurations can be stored and recalled. Selection is via the rear panel mode switch. The saved parameters are also automatically recalled during power-up initialization. There is no read or write data associated with this command.

Parameter: RECALL
Settings: None, command only
Type: Command

*Example:* **RECALL**

### 1.4.33. Parameter Dump (DUMP)

The Parameter Dump (DUMP) command causes the CLS-222 to return the entire current parameter set to the host computer. Information is displayed in both hexadecimal and decimal format. The dump data can be pasted into a file and used for subsequent download into the CLS-222. Note that the last two entries are read-only and should not be omitted from the file. A typical DUMP command response is shown below.

Parameter: DUMP
Settings: None, command only
Type: Command

*Example:* **DUMP**

*CLS-222 Dump Example:*

```
CL_MODE     0x00        / 0
CONTINUOUS  0x01        / 1
EXSYNC_ENB  0x00        / 0
EXSYNC_SEL  0x00        / 0
LINESCAN    0x00        / 0
FREQUENCY   0x32        / 50
LVAL_HI     0x0500      / 1280
LVAL_LO     0x0020      / 32
FVAL_HI     0x02D0      / 720
FVAL_LO     0x0010      / 16
FVAL_SETUP  0x08        / 8
FVAL_HOLD   0x08        / 8
DVAL_MODE   0x00        / 0
DVAL        0x01        / 1
CLK_DIS     0x00        / 0
X_STEP      0x01        / 1
Y_STEP      0x01        / 1
BAR_WIDTH   0xA0        / 160
BAYER_SEL   0x00        / 0
ROLL        0x00        / 0
A_PATSEL    0x03        / 3
B_PATSEL    0x00        / 0
C_PATSEL    0x00        / 0
D_PATSEL    0x00        / 0
E_PATSEL    0x00        / 0
F_PATSEL    0x00        / 0
G_PATSEL    0x00        / 0
```

```
H_PATSEL    0x00        / 0
I_PATSEL    0x00        / 0
J_PATSEL    0x00        / 0
A_FIXED     0x0000      / 0
B_FIXED     0x0000      / 0
C_FIXED     0x0000      / 0
D_FIXED     0x0000      / 0
E_FIXED     0x0000      / 0
F_FIXED     0x0000      / 0
G_FIXED     0x0000      / 0
H_FIXED     0x0000      / 0
I_FIXED     0x00        / 0
J_FIXED     0x00        / 0
A_INIT      0x0000      / 0
B_INIT      0x0000      / 0
C_INIT      0x0000      / 0
D_INIT      0x0000      / 0
E_INIT      0x0000      / 0
F_INIT      0x0000      / 0
G_INIT      0x0000      / 0
H_INIT      0x0000      / 0
I_INIT      0x00        / 0
J_INIT      0x00        / 0
AIA_TEST    0x00        / 0
AIA_SEL     0x00        / 0
POCL_MODE   0x00        / 0
POCL        0x00        / 0
CC          0x0F        / 15
VERSION     0x11        / 17
```

## 1.5. Specifications

**Table 1-4: CLS-222 Specifications**

| Feature | Specification |
|---|---|
| Video Interface | Camera Link v2.1 base/medium/full/72-bit/80-bit + PoCL |
| Video Connectors | 26-pin SDR/HDR type |
| Frequency Range | 10-95 MHz |
| Output Device | Texas Instruments DS90CR287 (per specification) |
| Serial Port | RS-232 male 9-pin D-Sub, modem cable included |
| Mode Switch | 4 position, Control and configuration select |
| Quick-Configuration SW | Windows XP, 7, 8, 10 |
| Power Supply | Universal wall style w/ outlet plug set |
| Power Jack | 2.1 x 5.5 mm, center-positive. Locking style optional |
| Power Requirements | 5 VDC, 700 mA typical |
| Cabinet Dimensions | 5.28” (L) x 1.18” (H) 7.12” (D) |
| Weight | 16 oz |
| Operating Temp Range | 0 to 50° C |
| Storage Temp Range | -25 to 75° C |
| Relative Humidity | 0 to 90%, non-condensing |

# 2. Interface

## 2.1. Front Panel Connections

The CLS-222 Camera Link Simulator front panel is shown in Figure 2-1. The front panel contains two 26-pin SDR/HDR (i.e. miniCL) connectors for connecting to the frame grabber. Camera Link "medium", "full", "72-bit", and "80-bit" configurations utilize both video connectors. "Base" configurations utilize only the "base" connector. The video connector and signal assignment complies with the Camera Link specification.

The "PWR" LED indicates the unit is on. The "OUT" LED indicates the unit is outputting video data.

The two PoCL LEDs, when illuminated, identify PoCL power presence at the respective connector.

*Note that the connector pin assignments are as defined for the camera interface in the Camera Link Specification.*

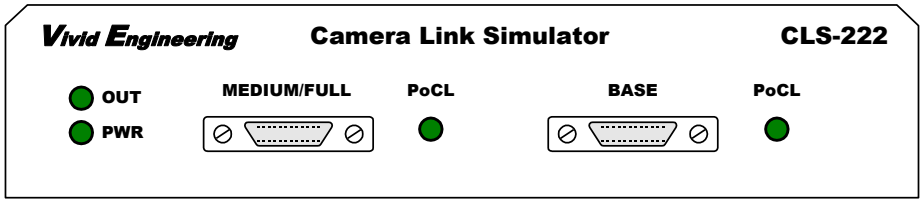



**Figure 2-1: CLS-222 Front Panel**

### 2.1.1. Cable Shield Grounding

Camera Link cable "outer" shields are connected to the CLS-222 aluminum case. The case is isolated from the CLS-222 circuitry and the cable "inner" shields.

The frame grabber cable "inner" shield connects to circuit digital ground, maintaining signal reference levels between the CLS-222 and the frame grabber.

## 2.2. Rear Panel

The CLS-222 Camera Link Simulator rear panel is shown in Figure 2-2. The rear panel contains an RS-232 connector, 4-position mode switch, on-off switch, and DC power jack.

The DC power jack accepts either a standard 2.1 x 5.5 mm barrel-style power plug or a special locking plug. The locking plug has bayonet-style "ears" on the barrel. Once inserted, the plug is turned ¼ turn clockwise. This locks the connection and provides retention. Plug polarity is center-positive. Recommended locking power plug is Philmore part number 2150 or Shogyo MP-121AR.

The RS-232 serial port connector is a standard 9-pin male D-Sub type (DB9). Connection to PC, USB adapter, etc is via a null-modem cable (included).

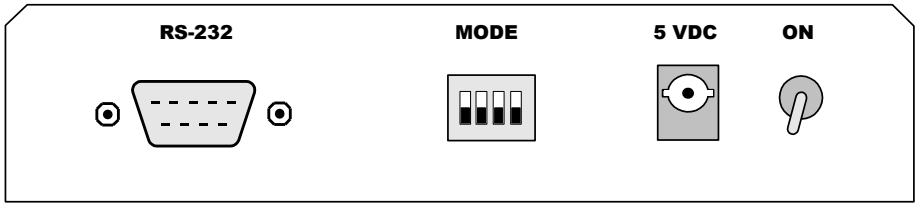



**Figure 2-2: CLS-222 Rear Panel**

# 3. Mechanical

## 3.1. Dimensions

The CLS-222 Camera Link Simulator cabinet dimensions are shown in Figure 3-1.

The CLS-222 is housed in a sturdy aluminum enclosure. The body is extruded aluminum, with detachable front and rear endplates. The enclosure incorporates a mounting flange. The flange contains four predrilled holes (0.15" diameter) for convenient equipment mounting. A mounting drawing is provided in Figure 3-2.

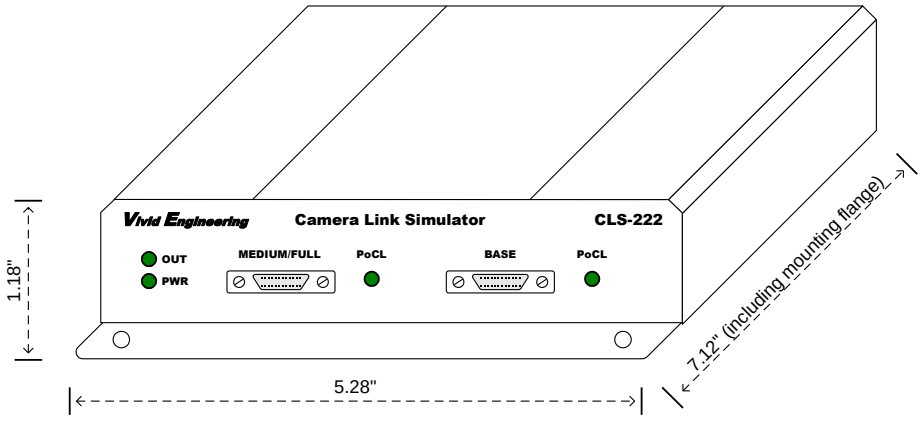



**Figure 3-1: CLS-222 Cabinet Dimensions**

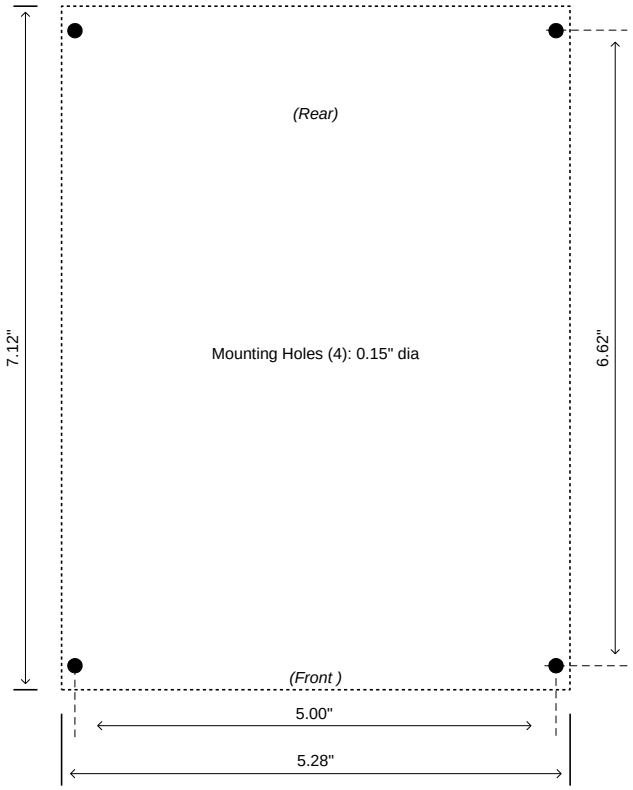



**Figure 3-2: Mounting Holes**

## 3.2. External Power Supply

The CLS-222 is powered by 5 VDC and incorporates a 2.1 x 5.5 mm DC power jack that accepts either a standard barrel-style power plug, or a special locking version. Power plug polarity is center-positive.

The CLS-222 includes a multi-nation wall-mount power supply that handles a wide power range (90-264 VAC, 47-63 Hz) and comes with a set of outlet plugs suitable for most countries (US, Europe, UK, etc). The CLS-222 may also be purchased with a locking-plug power supply, or without power supply.

# 4. Revision History

**Table 4-1: CLS-222 User's Manual Revision History**

| Document ID # | Date | Changes |
|---|---|---|
| 201432-0.1 | 9/23/2019 | Preliminary release of manual |
| 201432-0.2 | 7/28/2020 | Corrects Table 1-6 |
| | | |